

RUGGED SOLID-STATE RF AMPLIFIERS FOR ACCELERATOR APPLICATIONS – DESIGN AND PERFORMANCE FROM AN INDUSTRY PERSPECTIVE

Shane Dillon, Wilbert Gonzales, Brad Nobel, Janice Reid, Chris Schach,
Tomco Technologies, SA 5069, Australia.

Abstract

Recent advances in transistor technology are making solid-state RF amplifiers an increasingly viable alternative to tube systems in accelerator applications. This paper details the development and performance of a range of new high power amplifiers, based on current MOSFET technology, and designed specifically for this application. A generic modular architecture that can be used to construct high power CW amplifier systems operating from HF up to S-band, is detailed. Key design considerations in terms of modularity, redundancy, reliability and cost are discussed.

INTRODUCTION

The latest generation of LDMOS RF transistors potentially enable the construction of very high power RF amplifiers with excellent reliability and ruggedness, and a capital cost that competes favourably with vacuum tube technology. [1]

Our objective was to develop a range of high-power amplifiers to meet the diverse requirements encountered in accelerator applications. To minimise the amount of new design required to produce customised amplifiers, a generic design template was developed. The template includes a standardised chassis design, water cooling system, and protection and control systems. PA modules, drivers and combiners were designed for 500MHz and 800MHz, and amplifiers based on these were built and tested. S-band and L-band versions are currently under development.

SYSTEM DESCRIPTION

The amplifier system developed is based on a 19" rack-mount design, and uses a 5RU amplifier chassis as the system building block (or "power block"). Each power block contains eight PA (power amplifier) modules (figs. 1 and 2). The DC power supply is located in a separate 19" chassis, and contains hot-pluggable switchmode modules operating directly from a 3-phase mains supply.

Different PA modules are used at different operating frequencies but the mechanical footprint and control connections are preserved so that the chassis can be configured cost-effectively for different frequencies. The power rating per power block ranges from 1.5kW up to 6kW, depending on the frequency.

This architecture allows arbitrarily large systems to be constructed by repetition of the same basic power block. It provides easy serviceability and expandability, and reduces design costs, manufacturing costs and lead-time. Up to four power blocks can be combined in a single

rack. Multiple racks can be similarly combined to build systems of still higher power rating.

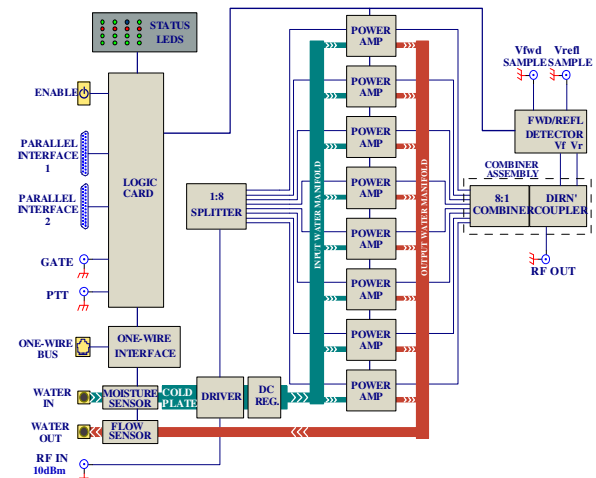


Figure 1: Block diagram applicable to all versions of the amplifier power block.

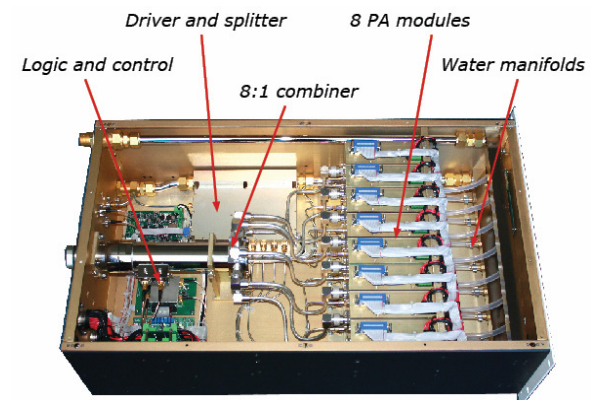


Figure 2: Internal layout of the 19" power block chassis (5kW CW, 500MHz), with 7-of-8 redundancy.

MAJOR DESIGN CONSIDERATIONS

Basic Building Block

A solid-state RF amplifier typically consists of a number of identical PA modules connected in parallel, and peripheral components such as drivers, protection/control circuits, splitters, combiners and PSU's. There are many possible ways in which these modules can be grouped together, with varying degrees of parallelism. Highly parallel systems with a lot of

redundancy are very reliable but their cost and complexity can be prohibitive. Highly serial systems are simpler and cheaper but, due to their reduced redundancy, their reliability may be compromised. The optimum architecture lies between these two extremes, with PA's grouped into blocks. The chosen configuration of eight PA's per power block is a best-fit solution based on:

- Reliability - a useful but economical base level of true redundancy must be built into the design.
- Power density- must be high enough to achieve cost targets and give a suitably sized power increment.
- Serviceability – the amplifier chassis must be physically manageable, setting a weight limit of about 40kg

Reliability and Redundancy

It is often stated that modular, solid-state amplifiers inherently contain redundancy because they can continue to operate if one or more of their parallel modules fail. However, this does not constitute true redundancy if the system is unable to produce the required power level under such partial failure conditions.

Redundancy must be designed in, and choosing the right level of redundancy is a cost/benefit problem. A comparison of cost versus reliability of various possible arrangements led to the use of "7-of-8" redundancy (the power block can still produce full power if one of its eight PA modules fails). To compare the relative cost/benefit of different levels of redundancy, simple static reliability analysis was applied, whereby the reliability of a "k of n" redundant system, over a time period t, is given by:

$$R(t) = \sum_{j=k}^n C_k^n p(t)^j (1-p(t))^{n-j}$$

where R=parallel system reliability, p=module static reliability, C_k^n = binomial probability distribution. [2]

For a single 500MHz PA module, the static reliability over 5 years is 0.96 (calculated using the theoretical MTBF and assuming an exponential reliability function). This gives an 8-module parallel system reliability of $R(t) = 0.73$ without redundancy, compared to $R(t) = 0.97$ with 7-of-8 redundancy. This is equivalent to a factor of 8 improvement in MTBF, indicating that 7-of-8 redundancy provides a significant improvement in reliability.

If one of the eight modules fails, the remaining seven must each be capable of producing approximately 1dB of additional power (factoring in power dissipation in the combiner). To achieve this, the amplifier's DC rail is normally set about 15% below full voltage. If a module fails, the DC rail is switched up to maximum and full output power is restored. Thus, in normal operation the PA modules operate on reduced voltage, leading to significantly reduced heat dissipation, reduced die temperature and, hence, extended MTTF.

A further advantage of grouping in this way is that the redundancy level is maintained as the system is expanded: a system containing eight 8-module power blocks can continue to produce full power if up to eight modules fail, regardless of their location in the system.

Figure 3 compares power sweeps under normal and partial failure conditions (one PA module unplugged), for a 500MHz, 5kW amplifier with 7-of-8 redundancy. Gain/phase linearity and output power capability are preserved, with only a slight change in the shape of the characteristic due to the shift in the transistor operating point. Note: for easier comparison the gain of the amplifier has been increased by 1dB in the 7-of-8 case so that the plots overlay.

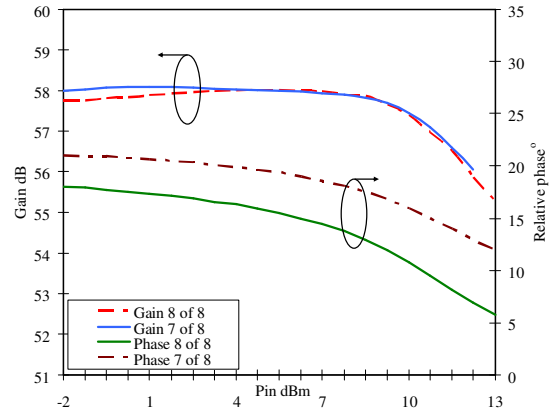


Figure 3: Gain and phase sweeps under normal and simulated partial failure conditions.

Thermal Considerations

Making use of the very high power density available from the new LDMOS transistors demands a very efficient cooling system. Transistor data typically show that the MTTF can drop by a factor of almost 2 for every 10°C increase in die temperature.

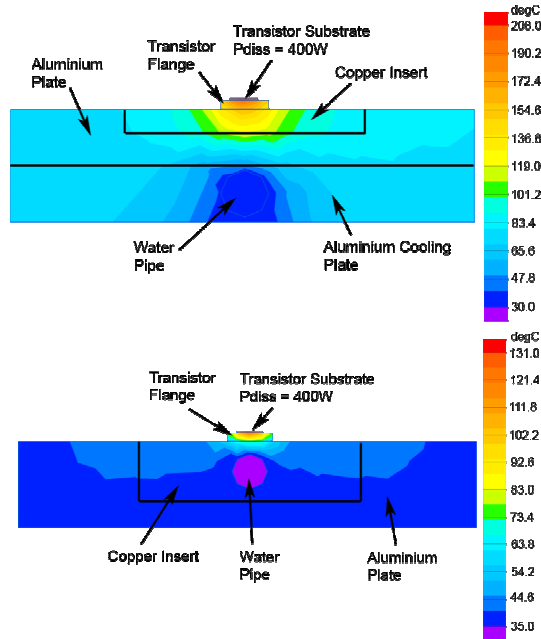


Figure 4: Finite element models of two possible transistor cooling arrangements.

Many different cooling plate designs were considered. Figure 4 compares finite element models of two candidate designs. In the first, the PA is bonded to a copper heat spreader in an aluminium enclosure, which is then bolted to a commercial cold-plate. In the second (the one finally selected), the transistor is directly bonded to a copper water jacket so that thermal resistance is kept to an absolute minimum. Direct infra-red measurements of die temperature under RF operation verified the predicted performance and showed that for 400W heat dissipation, the die was held at less than 100 degrees above the water temperature. At that temperature the MTTF of an LDMOS transistor is typically over 1000 years.

Measurements were also made of thermal resistance as a function of water flow rate for various cooling tube geometries to ensure that turbulent flow is maintained through the cooling tubes over the full range of flow rates.

Efficiency

LDMOS transistors can provide excellent efficiency, but it is optimum only when the transistor is operating close to saturation. Since the saturation point approximately follows the DC supply voltage, a system was developed to allow the DC supply to be remotely adjusted to provide good efficiency and linearity over a range of different power levels.

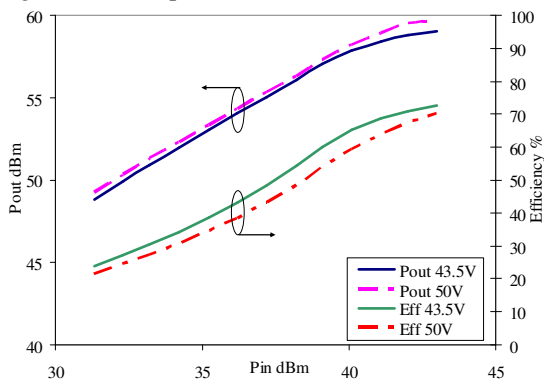


Figure 5: 500MHz PA module power and efficiency at two different DC supply voltages.

Remote Control and Monitoring Interface

The control and monitoring interface is a parallel type so that all of the status outputs and control inputs are available simultaneously. This avoids the complexity and time lag of a serial interface and provides maximum flexibility to the end-user.

A secondary interface, using a standard one-wire serial protocol provides detailed but non-critical information for individual modules such as temperature, forward and reflected voltage and DC current draw.

Pulsed Operation

The amplifiers include high-speed RF gating and bias switching, to provide inter-pulse noise blanking under pulsed operation. The pulsed output shows very fast rise and fall times and is free from ringing or overshoot.

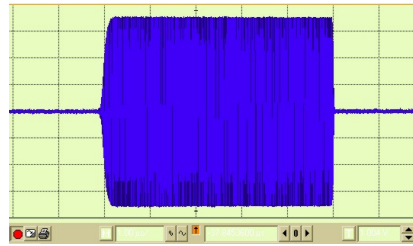


Figure 6: Pulsed operation. 5µs pulse width, 500MHz, 5kW PEP. 1µS/div.

Protection Systems

The amplifier system must be extremely robust and tolerate, without damage, conditions such as infinite output mismatch, out-of-band or over-driven input signals, condensation and cooling water faults.

Protection against inadequate cooling is provided by thermal switches closely coupled to the transistors. This was chosen in preference to reliance on flow sensors, which do not directly ensure that temperatures are within safe limits. Infinite load mismatch is handled through the use of a circulator and termination inside each PA module. The circulator and its load are rated to withstand high peak power transient reflections such as those encountered in an arc event. The system is also able to provide a level of protection to the load connected to its output through a user adjustable ALC (Automatic Level Control) on both the forward and reflected output levels.

SUMMARY

A generic power amplifier design has been developed addressing the technical and commercial challenges involved in making best use of the new LDMOS transistors. The design incorporates 7-of-8 redundancy which significantly enhances reliability without adding unacceptable cost overheads, and ensures that output power and linearity are retained under partial failure conditions. 500MHz and 800MHz versions have been developed. L-band and S-band versions are under development.

REFERENCES

- [1] Marco Di Giacomo, "Solid State RF Amplifiers for Accelerator Applications", PAC'09, Vancouver, 5th May 2009, TU4RAI01.
- [2] B. S. Dhillon, "Reliability, Quality, and Safety for Engineers", Chapter 4, CRC Press 2005, ISBN: 978-0-8493-3068-1